ABSTRACT OF THE DISCLOSURE

A memory device with vertical transistors and deep trench capacitors. The device includes a substrate containing at least one deep trench and a capacitor deposited in the lower portion of the deep trench. A conducting structure, having a first conductive layer and a second conductive layer, is deposited on the trench capacitor. A ring shaped insulator is deposited on the sidewall and between the substrate and the first conductive layer. The first conductive layer is surrounded by the ring shaped insulator, and the second conductive layer is deposited on the first conductive layer and the ring shaped insulator. A diffusion barrier between the second conductive layer and the substrate of the deep trench is deposited on one side of the sidewall of the deep trench. A TTO is deposited on the conducting structure. A control gate is deposited on the TTO.